Fig. 1

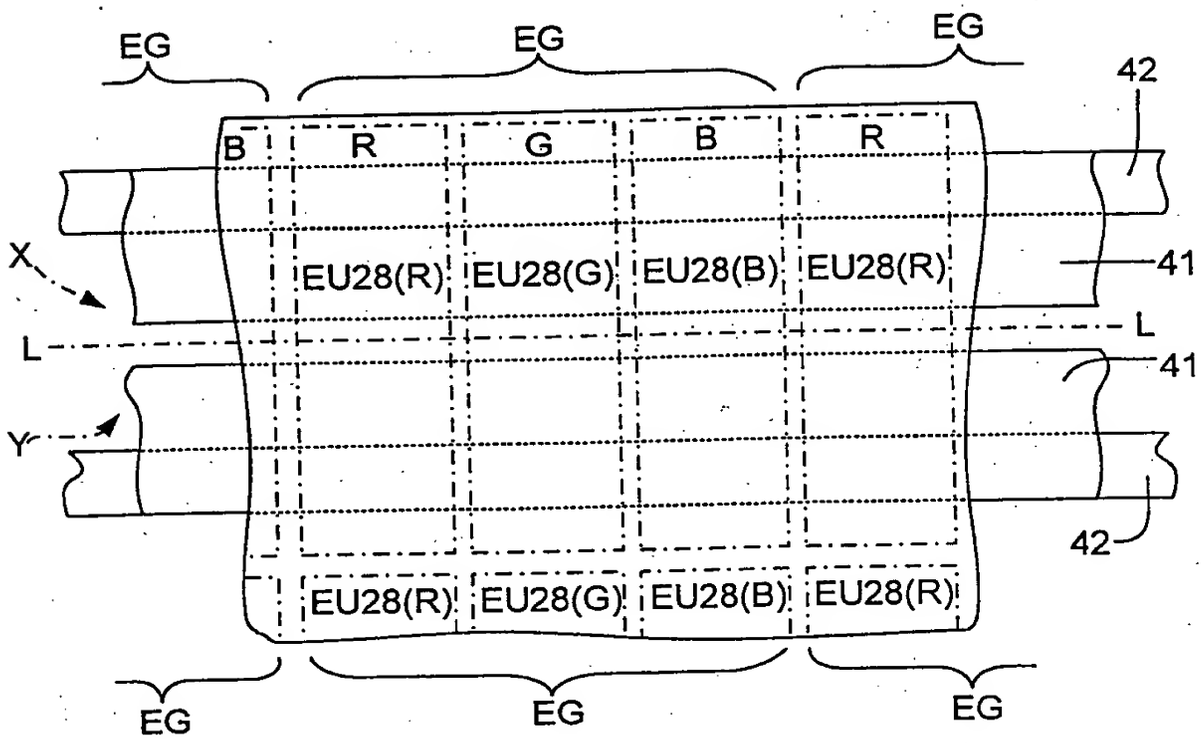
EG
EG
EG
42
B
R
G
B
R
X
EU28(R)
EU28(G)
EU28(B)
EU28(R)
41
L
L
41
Y
42
EU28(R)
EU28(G)
EU28(B)
EU28(R)
EG
EG
EG

Fig.2

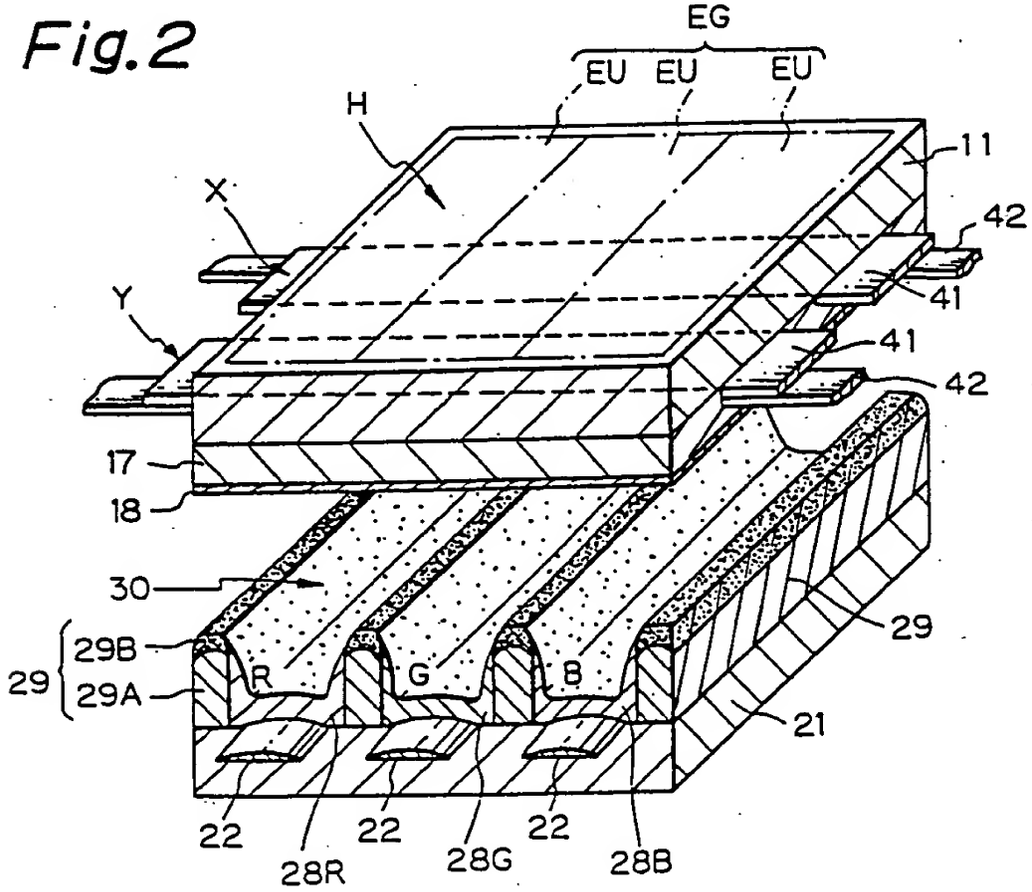
EG
EU
EU
EU
H
11
X
42
41
Y
41
42
17
18
30
29
29B
29A
R
G
B
21
22
22
22
28R
28G
28B

Fig.3A PRIOR ART

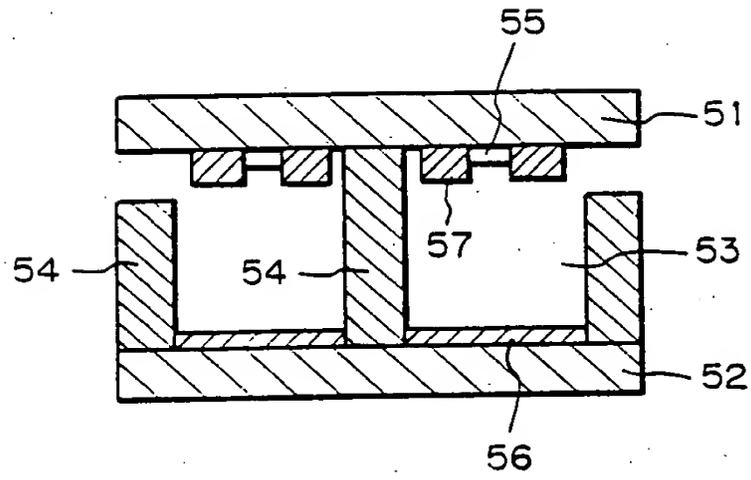

Fig.3B PRIOR ART

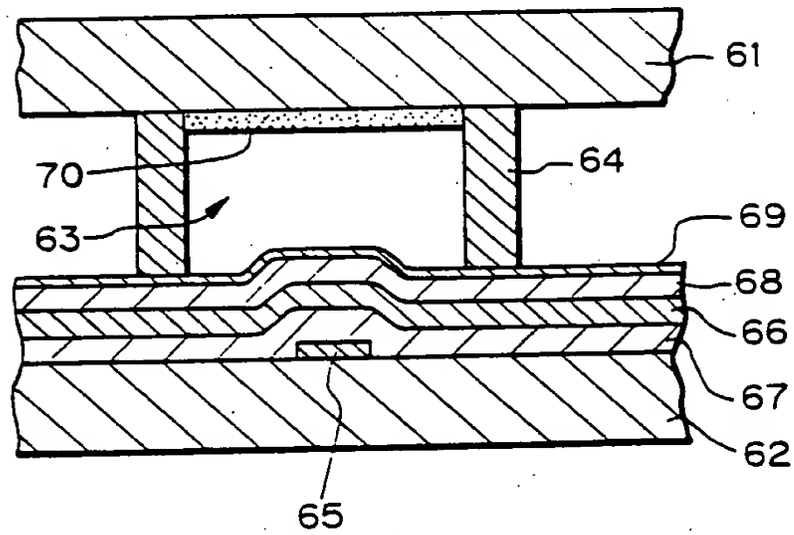

Fig. 4 PRIOR ART

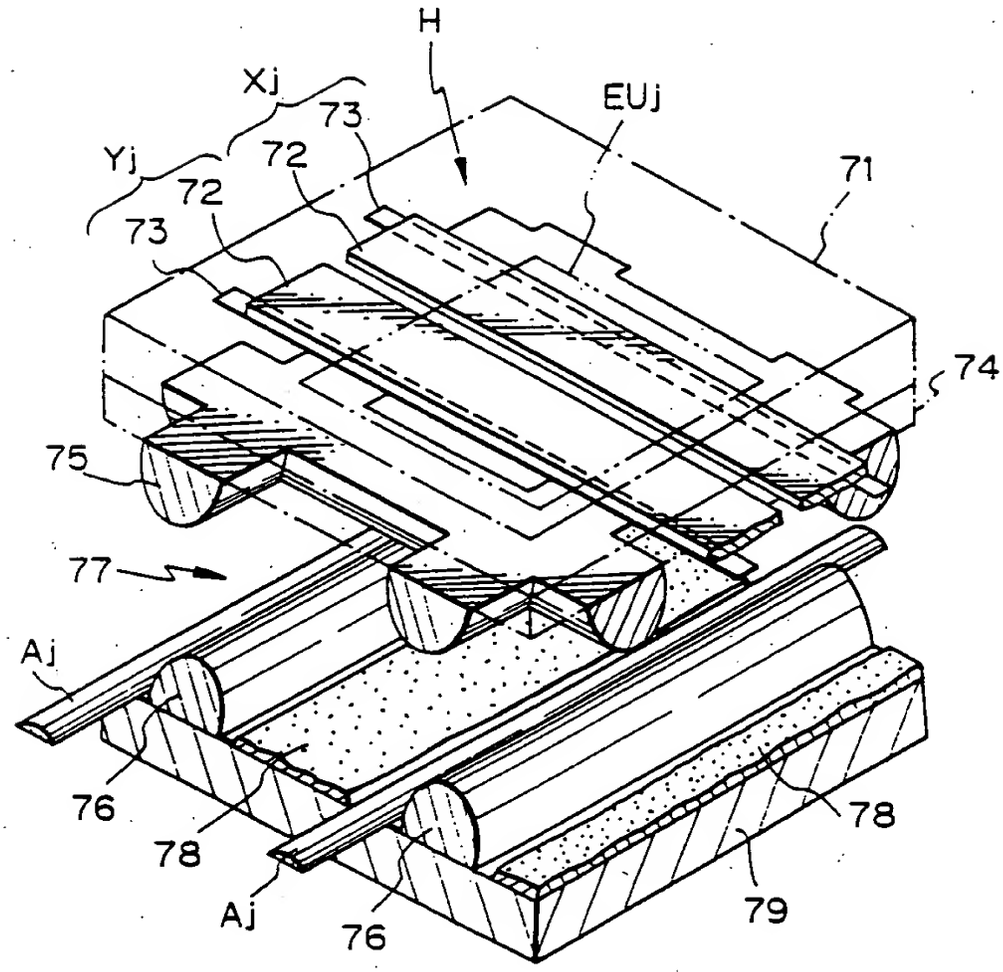

Fig. 5 PRIOR ART

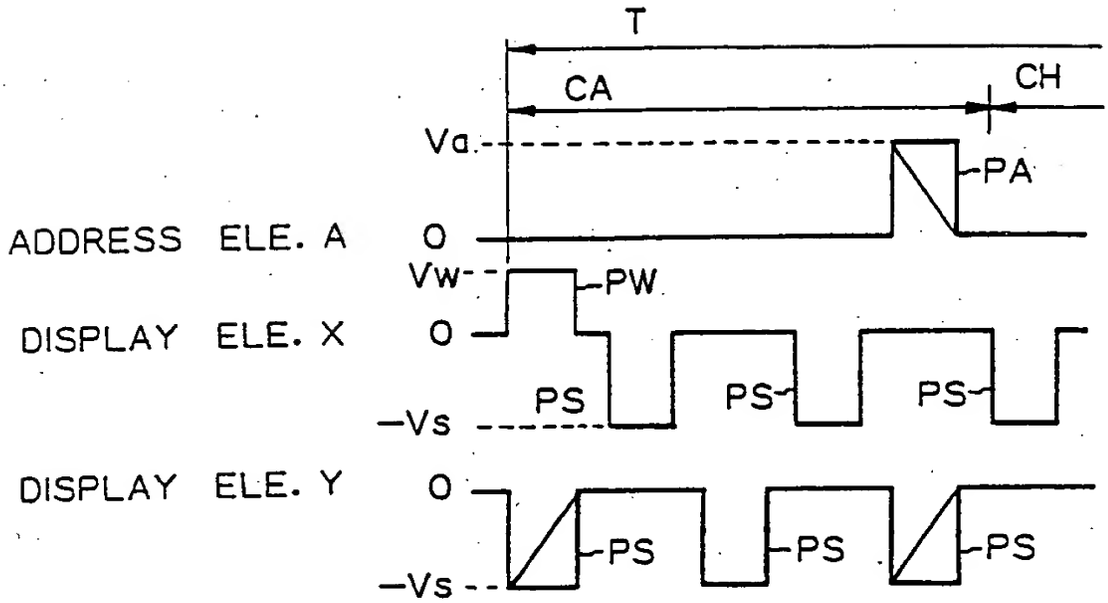

Fig. 6
PRIOR ART

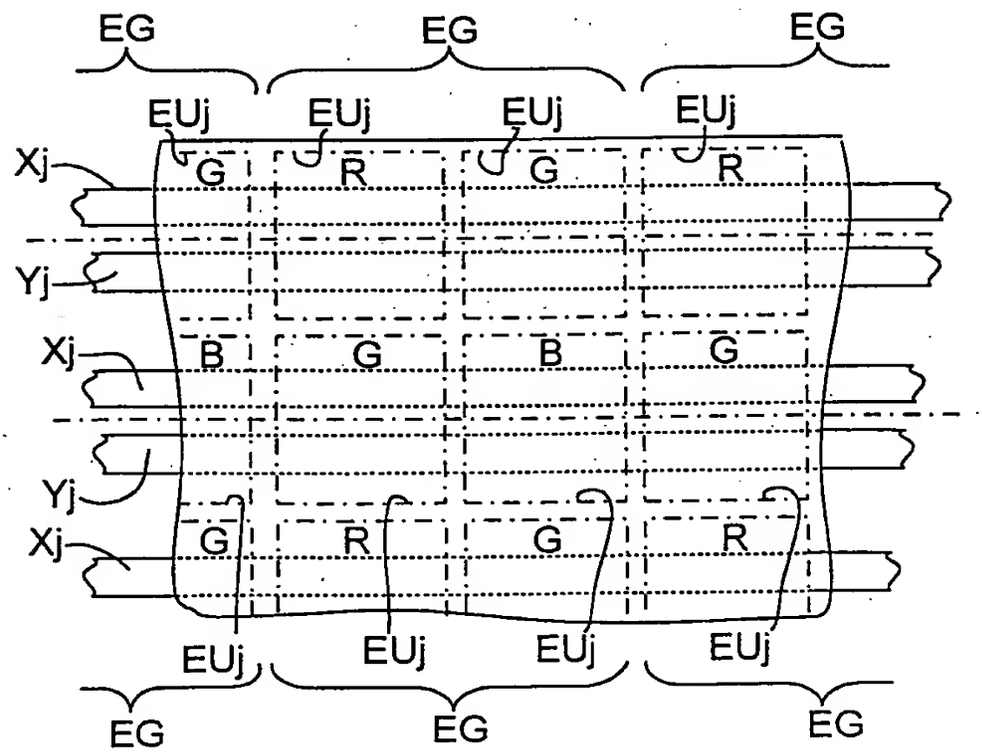

Fig. 7

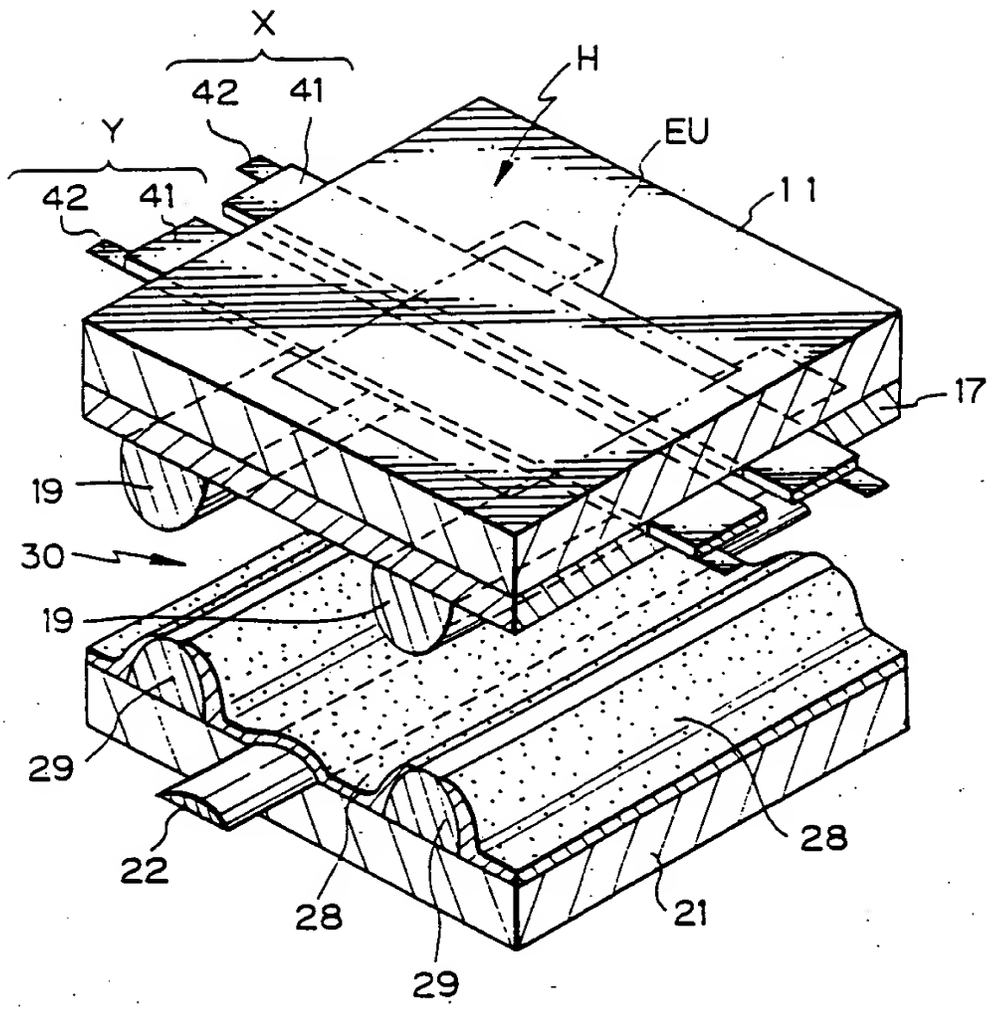

Fig. 8

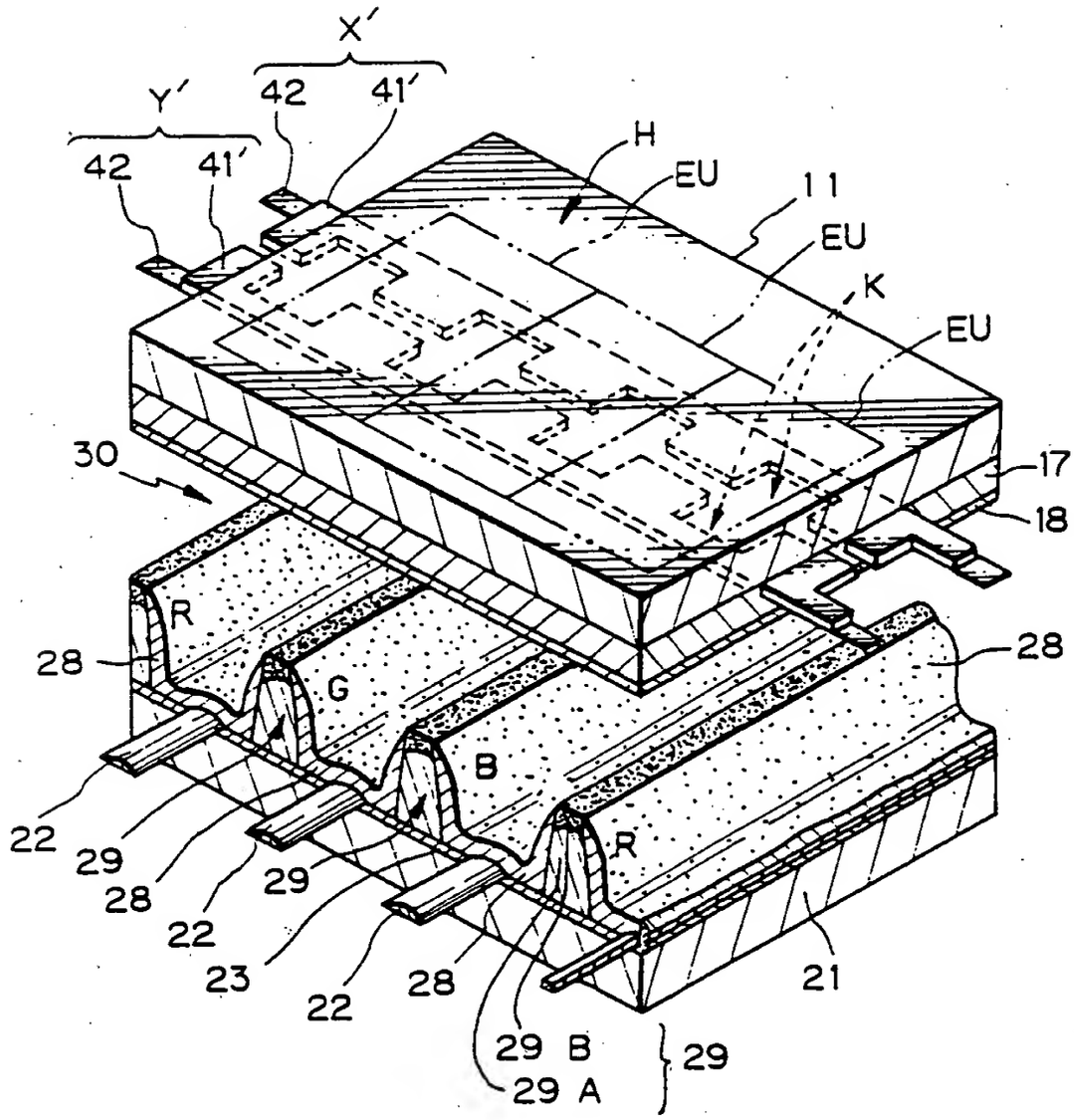
X'
Y'
42
41'
42
41'
H
EU
11
EU
K
EU
30
17
18
R
28
G
28
B
22
29
28
22
29
R
23
22
28
21
29 B
29 A
29

Fig. 9

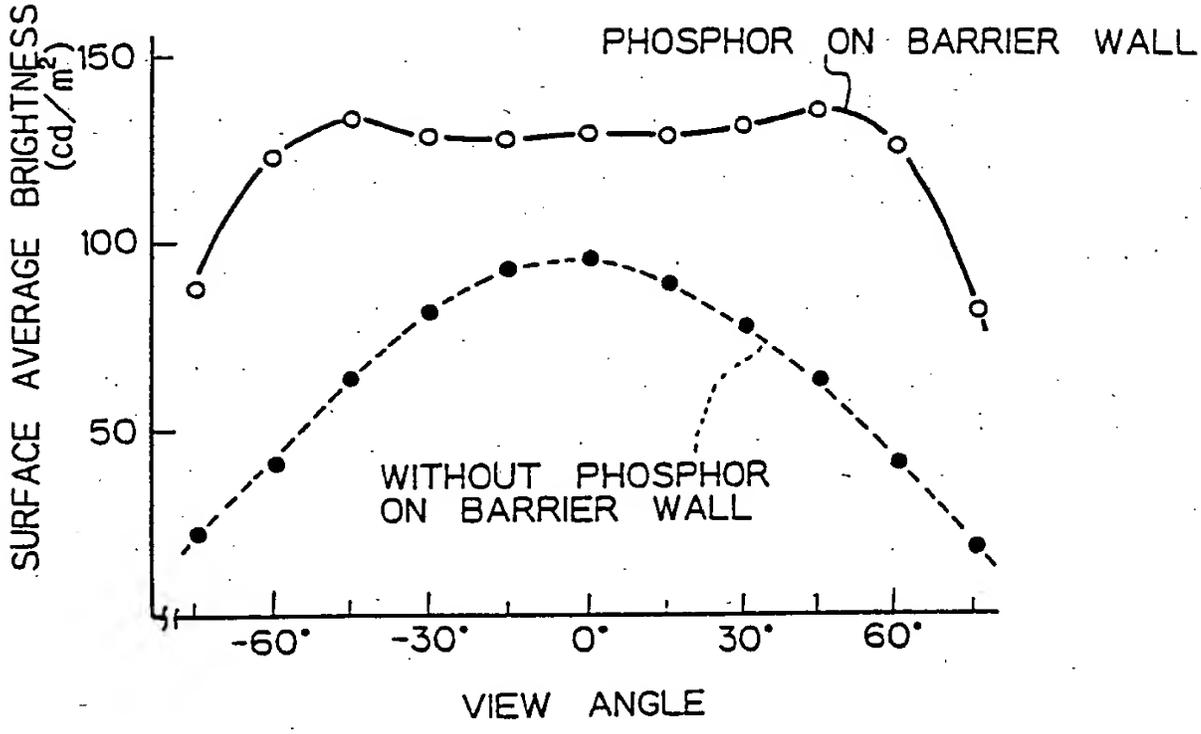
SURFACE AVERAGE BRIGHTNESS (cd/m²)
150
100
50
PHOSPHOR ON BARRIER WALL
WITHOUT PHOSPHOR ON BARRIER WALL
-60°
-30°
0°
30°
60°
VIEW ANGLE

Fig. 10

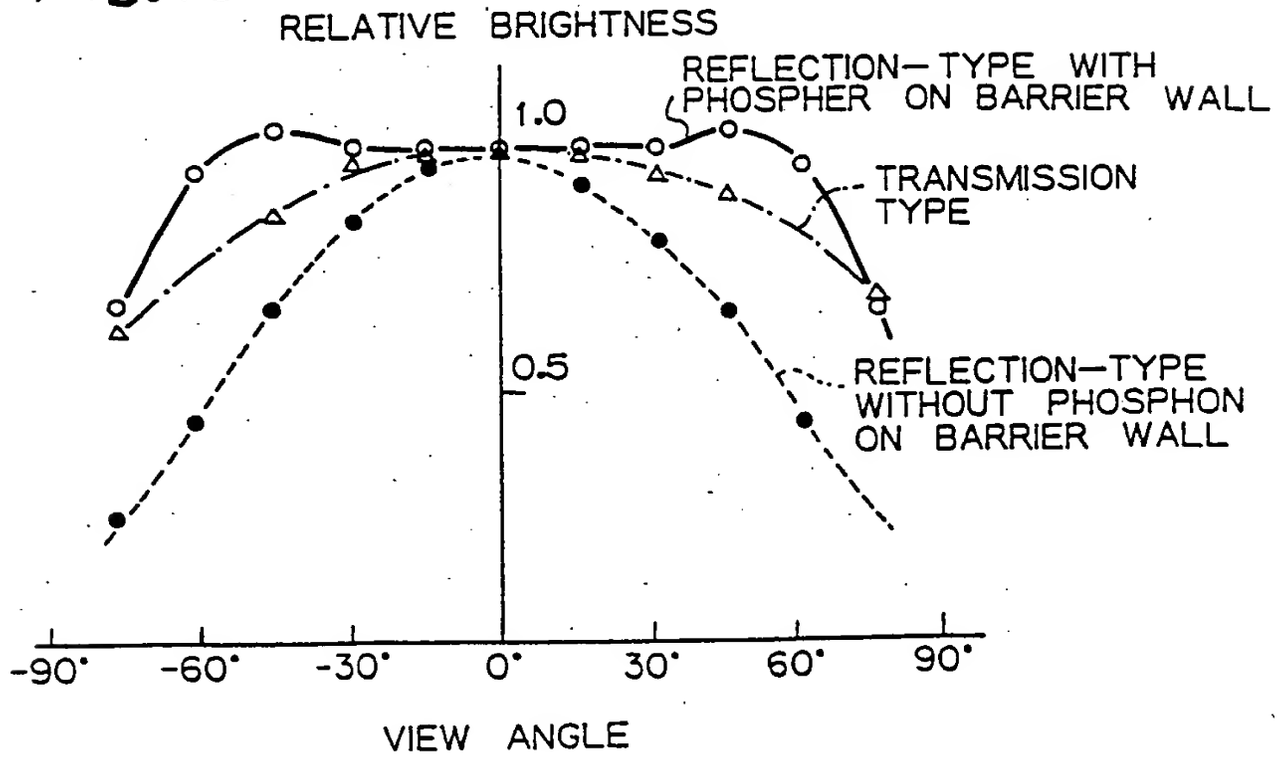
RELATIVE BRIGHTNESS
1.0
0.5
REFLECTION—TYPE WITH PHOSPHER ON BARRIER WALL
TRANSMISSION TYPE
REFLECTION—TYPE WITHOUT PHOSPHON ON BARRIER WALL
-90°
-60°
-30°
0°
30°
60°
90°
VIEW ANGLE

Fig.11

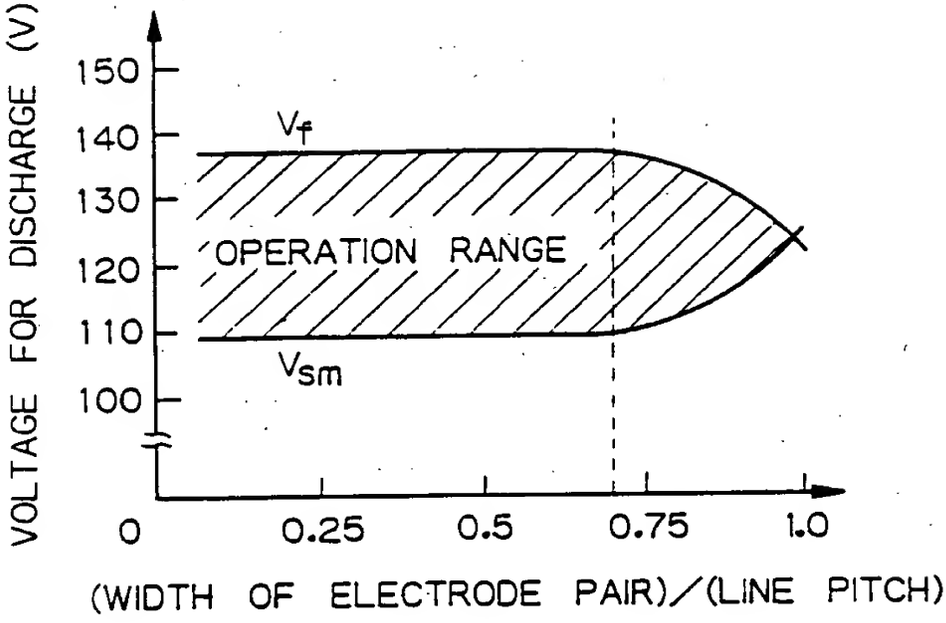
VOLTAGE FOR DISCHARGE (V)
150
140
130
120
110
100
Vf
OPERATION RANGE
Vsm
0
0.25
0.5
0.75
1.0
(WIDTH OF ELECTRODE PAIR)/(LINE PITCH)

Fig.12

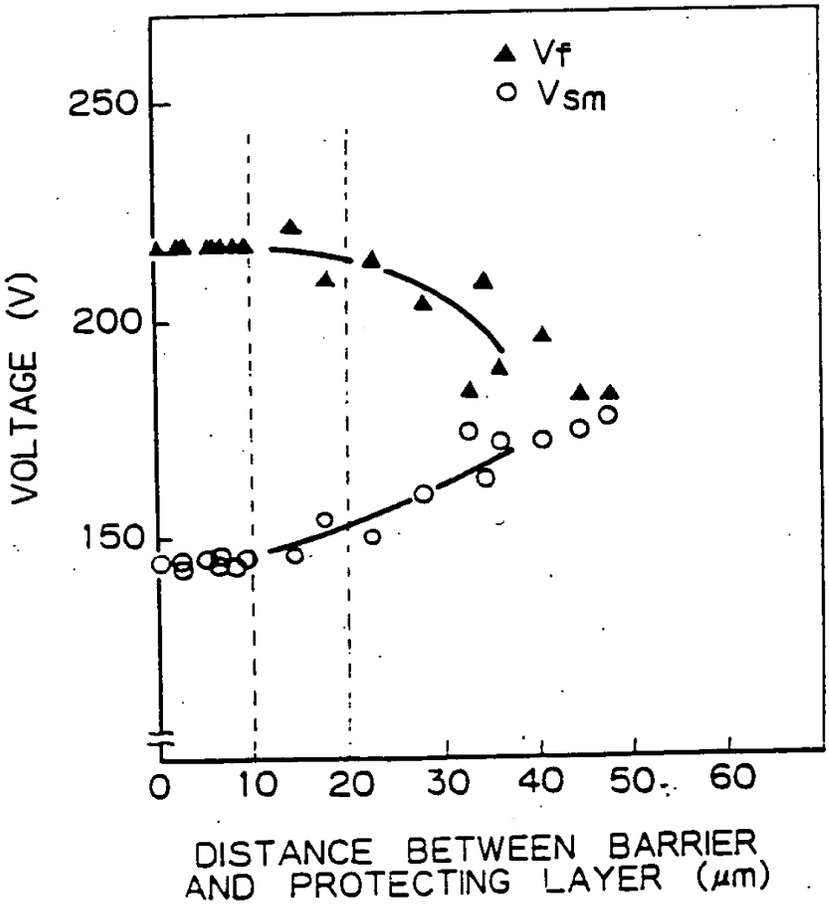
▲ Vf
○ Vsm
VOLTAGE (V)
250
200
150
0
10
20
30
40
50
60
DISTANCE BETWEEN BARRIER AND PROTECTING LAYER (μm)

Fig. 13

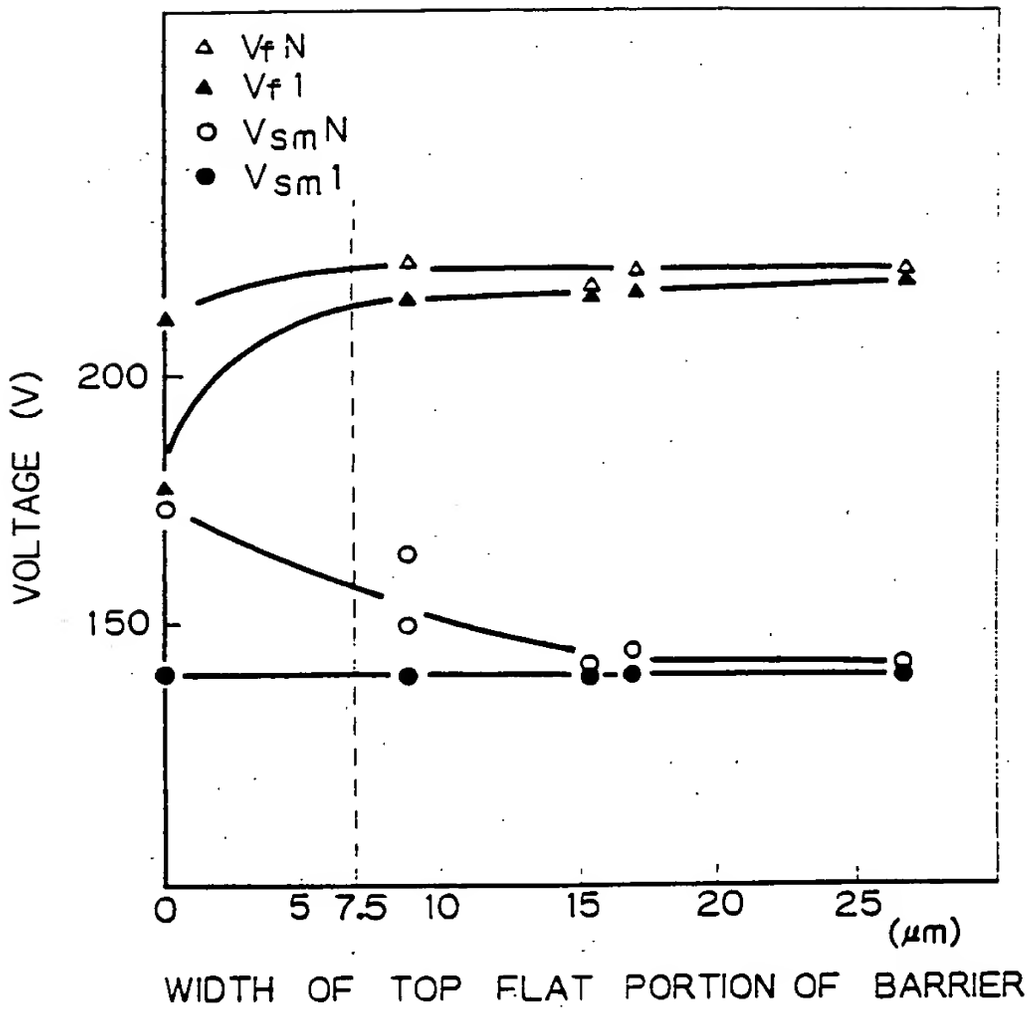
Vf N
Vf 1
Vsm N
Vsm 1
VOLTAGE (V)
200
150
0
5
7.5
10
15
20
25
(μm)
WIDTH OF TOP FLAT PORTION OF BARRIER

Fig.14

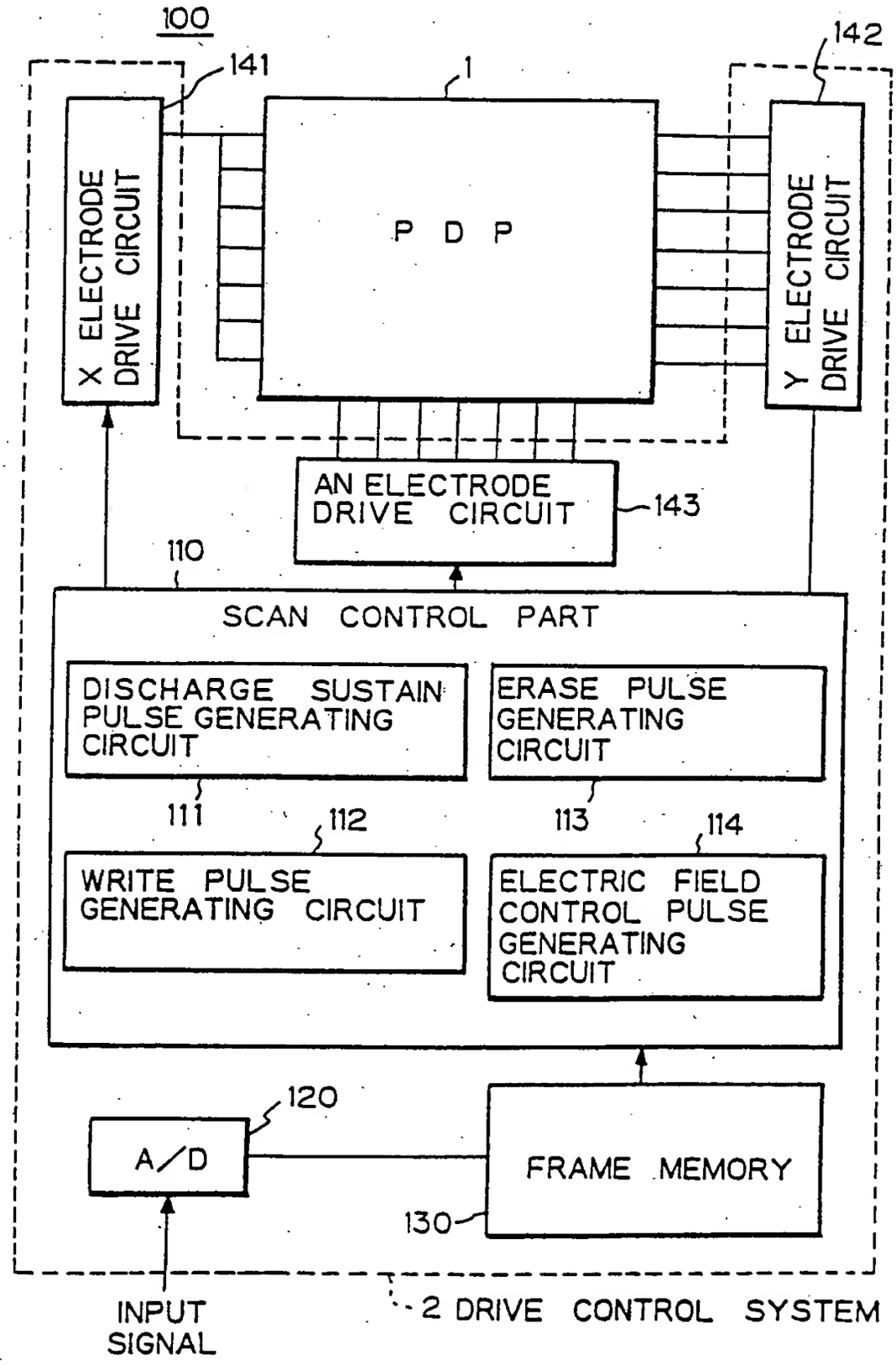
100
141
1
142
X ELECTRODE DRIVE CIRCUIT
P D P
Y ELECTRODE DRIVE CIRCUIT
AN ELECTRODE DRIVE CIRCUIT
143
110
SCAN CONTROL PART
DISCHARGE SUSTAIN PULSE GENERATING CIRCUIT
ERASE PULSE GENERATING CIRCUIT
111
112
113
114
WRITE PULSE GENERATING CIRCUIT
ELECTRIC FIELD CONTROL PULSE GENERATING CIRCUIT
120
A/D
FRAME MEMORY
130
INPUT SIGNAL
2 DRIVE CONTROL SYSTEM

Fig.15

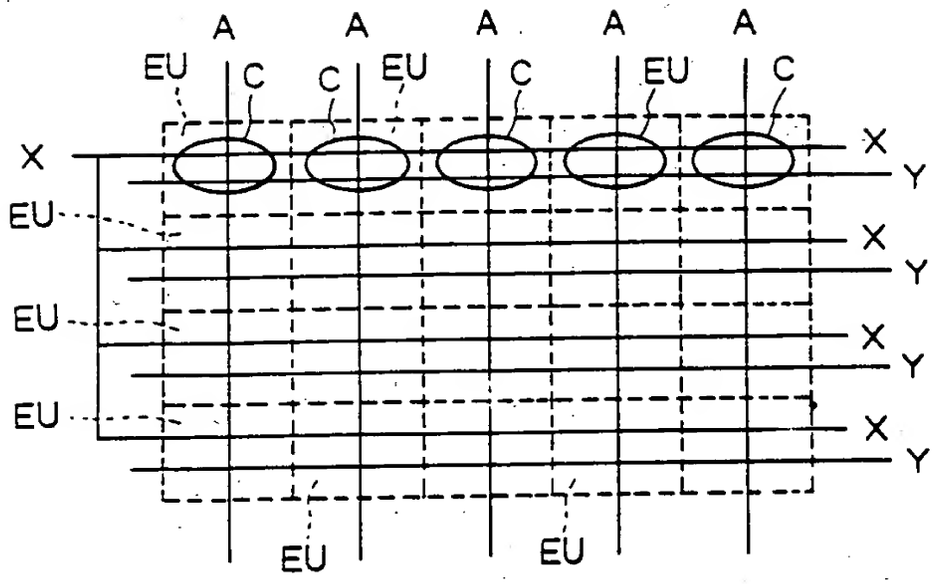
A
A
A
A
A
EU
C
C
EU
C
EU
C
X
Y
EU
EU
EU

Fig.16

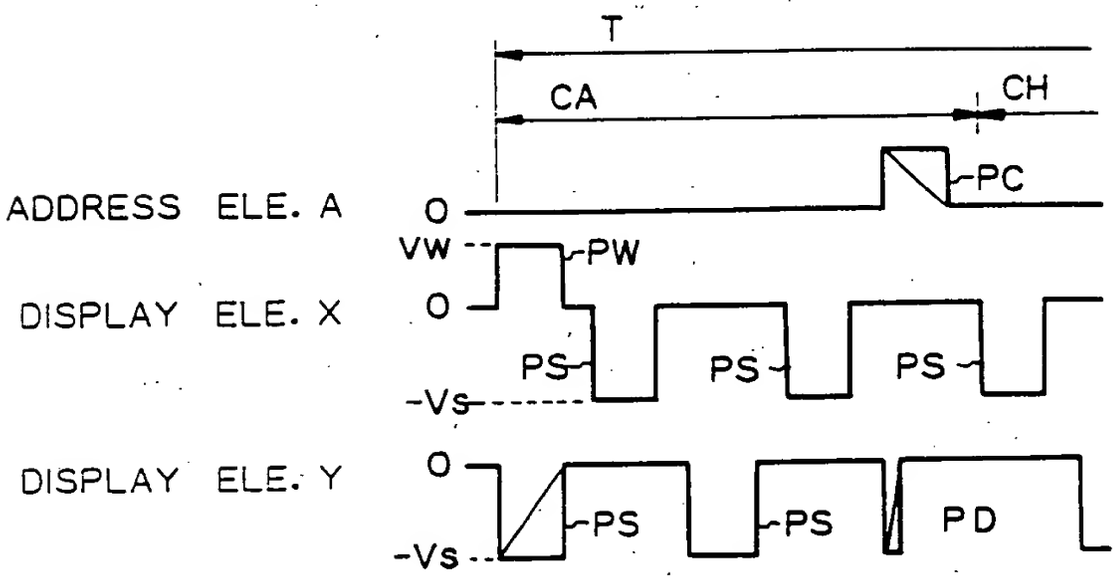
T
CA
CH
PC
ADDRESS ELE. A
O
VW
PW
DISPLAY ELE. X
O
PS
PS
PS
-Vs
DISPLAY ELE. Y
O
PS
PS
PD
-Vs

Fig.17

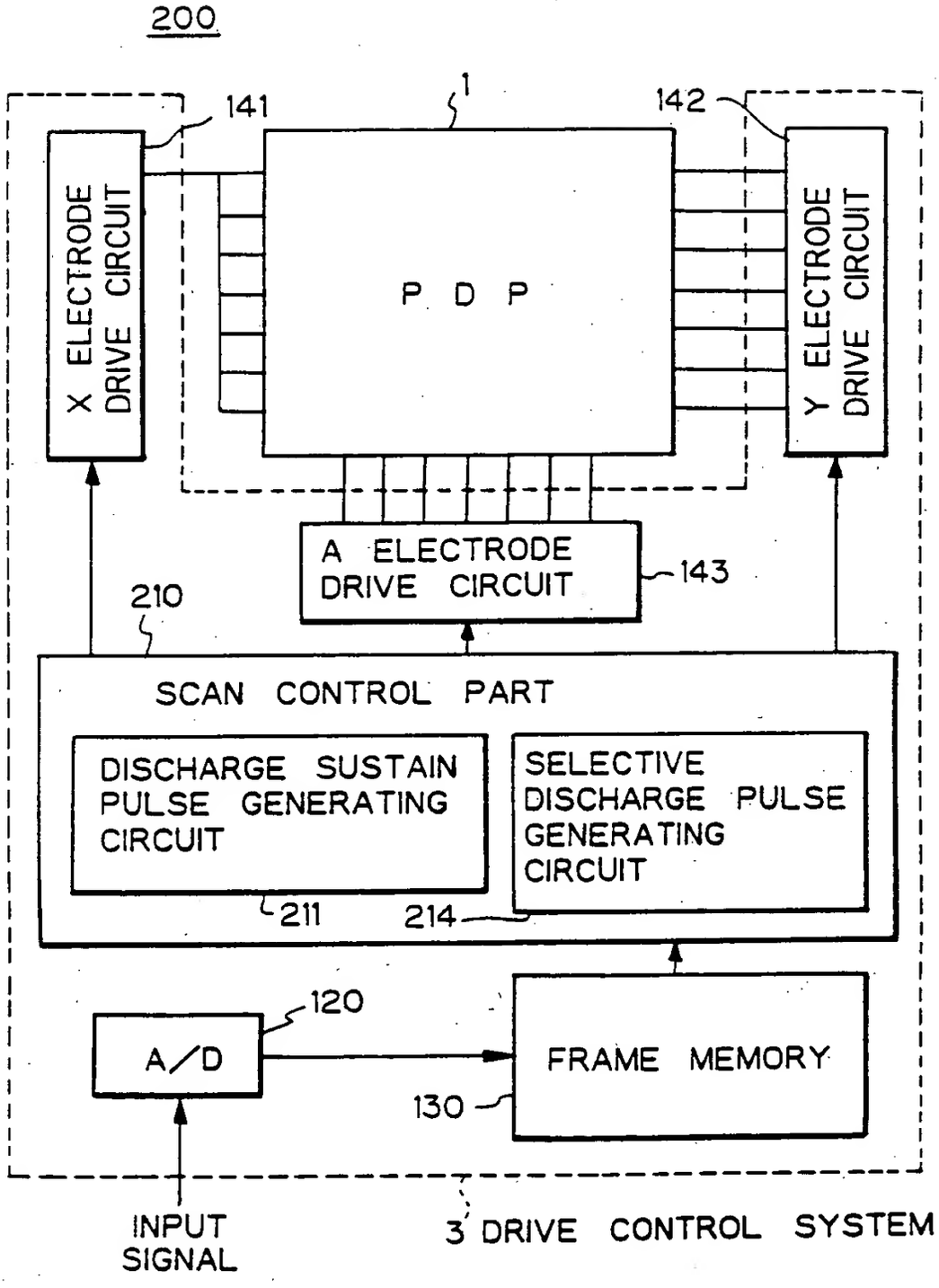
200
141
1
142
X ELECTRODE DRIVE CIRCUIT
P D P
Y ELECTRODE DRIVE CIRCUIT
A ELECTRODE DRIVE CIRCUIT
143
210
SCAN CONTROL PART
DISCHARGE SUSTAIN PULSE GENERATING CIRCUIT
SELECTIVE DISCHARGE PULSE GENERATING CIRCUIT
211
214
120
A/D
FRAME MEMORY
130
INPUT SIGNAL
3 DRIVE CONTROL SYSTEM

Fig.18

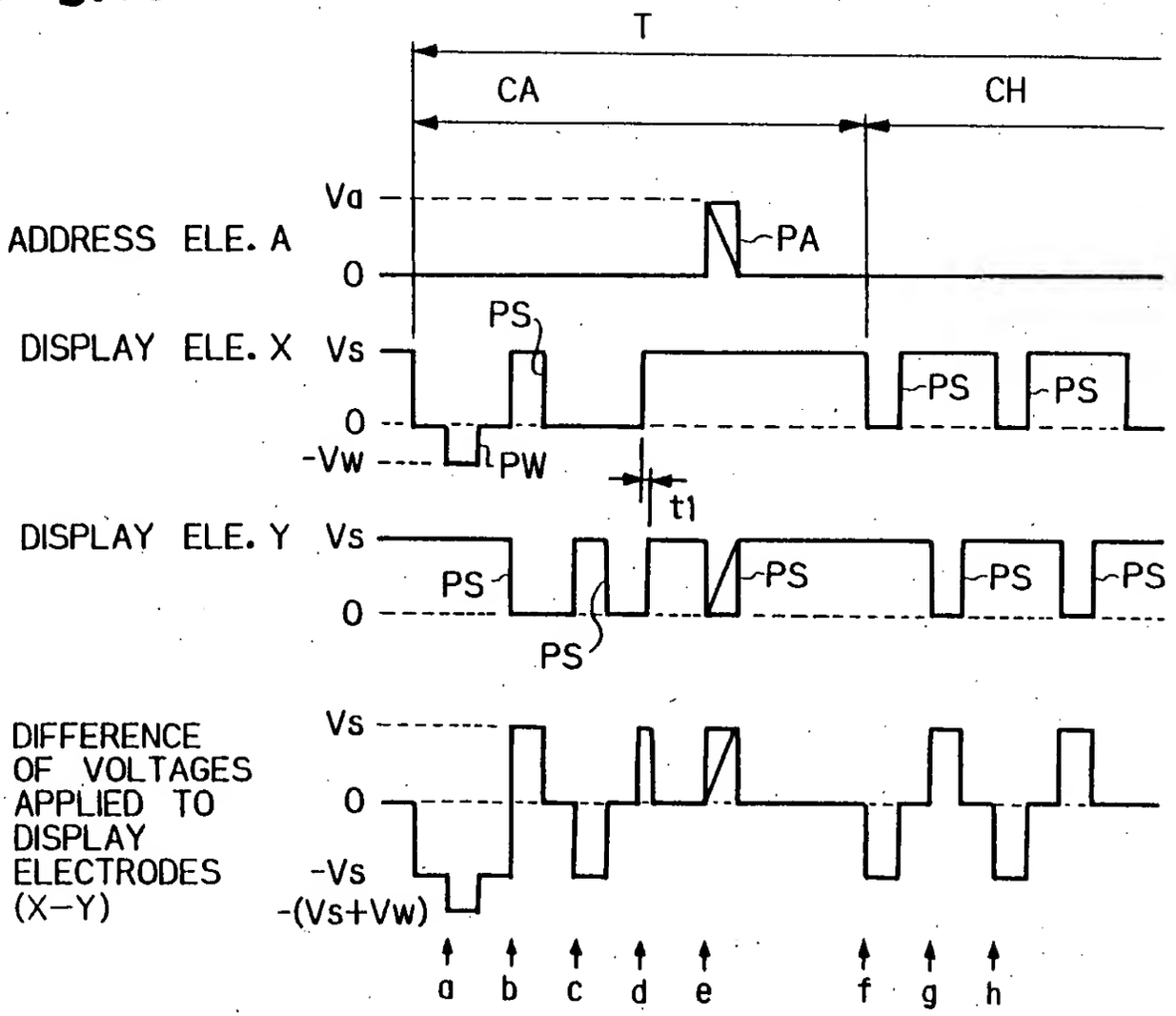
T
CA
CH
Va
ADDRESS ELE. A
0
PA
PS
DISPLAY ELE. X
Vs
0
-Vw
PW
PS
PS
t1
DISPLAY ELE. Y
Vs
0
PS
PS
PS
PS
PS
DIFFERENCE OF VOLTAGES APPLIED TO DISPLAY ELECTRODES (X-Y)
Vs
0
-Vs
-(Vs+Vw)
a
b
c
d
e
f
g
h

Fig.19A

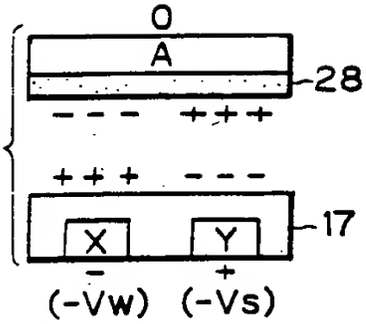

Fig.19B

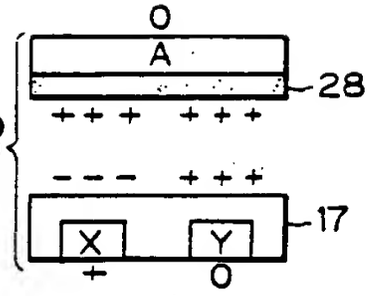

Fig.19C

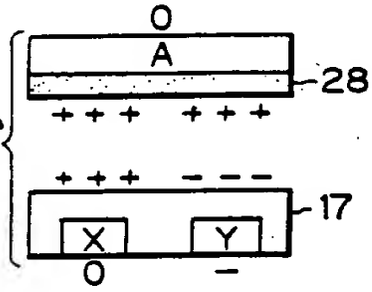

Fig.19D

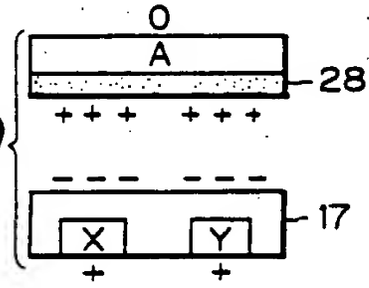

Fig.19E

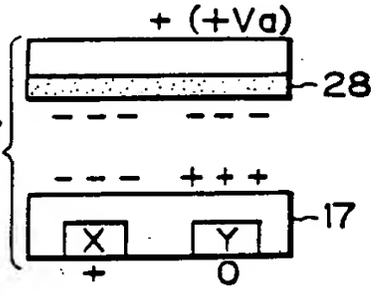

Fig.19F

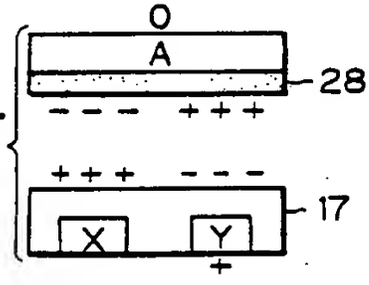

Fig.19G

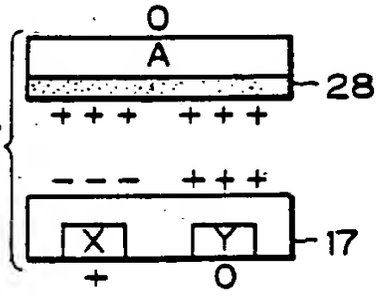

Fig.19H

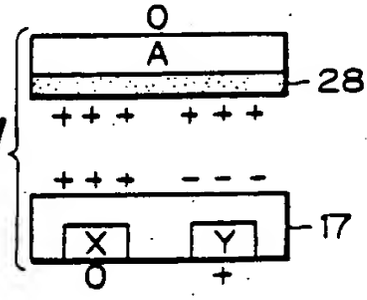

Fig.20

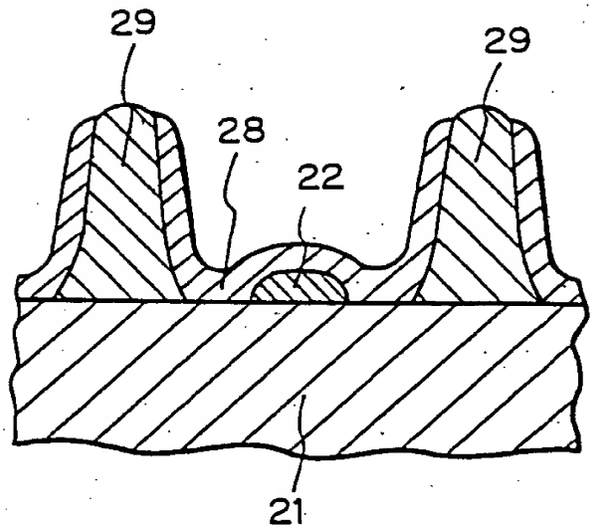
29
29
28
22
21

Fig.21

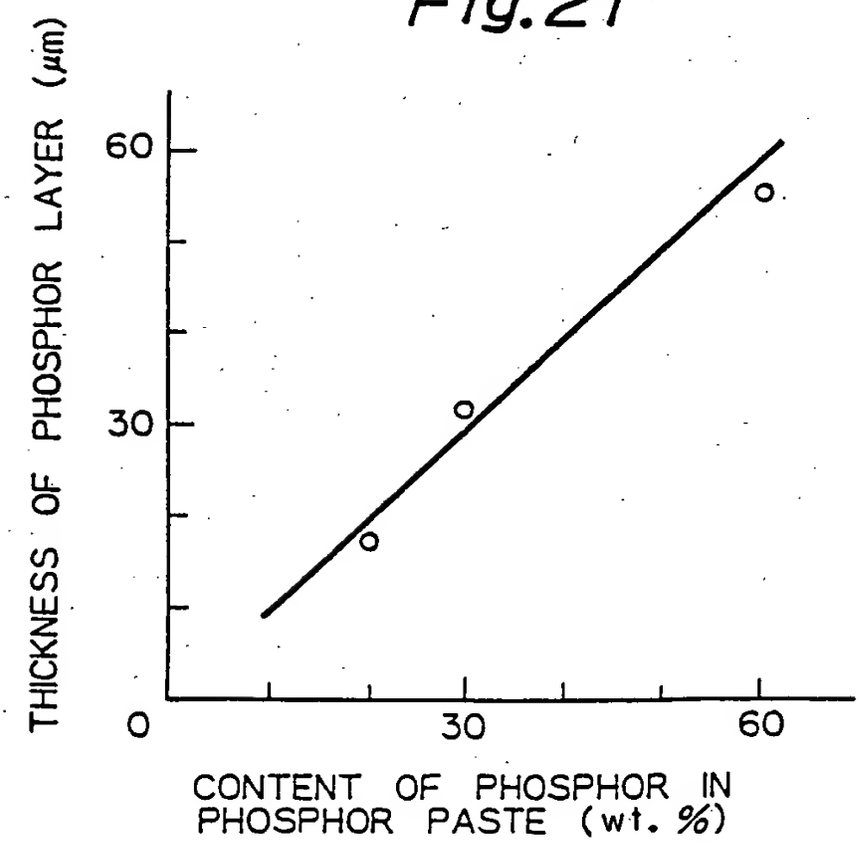
THICKNESS OF PHOSPHOR LAYER (μm)
60
30
0
30
60
CONTENT OF PHOSPHOR IN PHOSPHOR PASTE (wt. %)

Fig. 22A

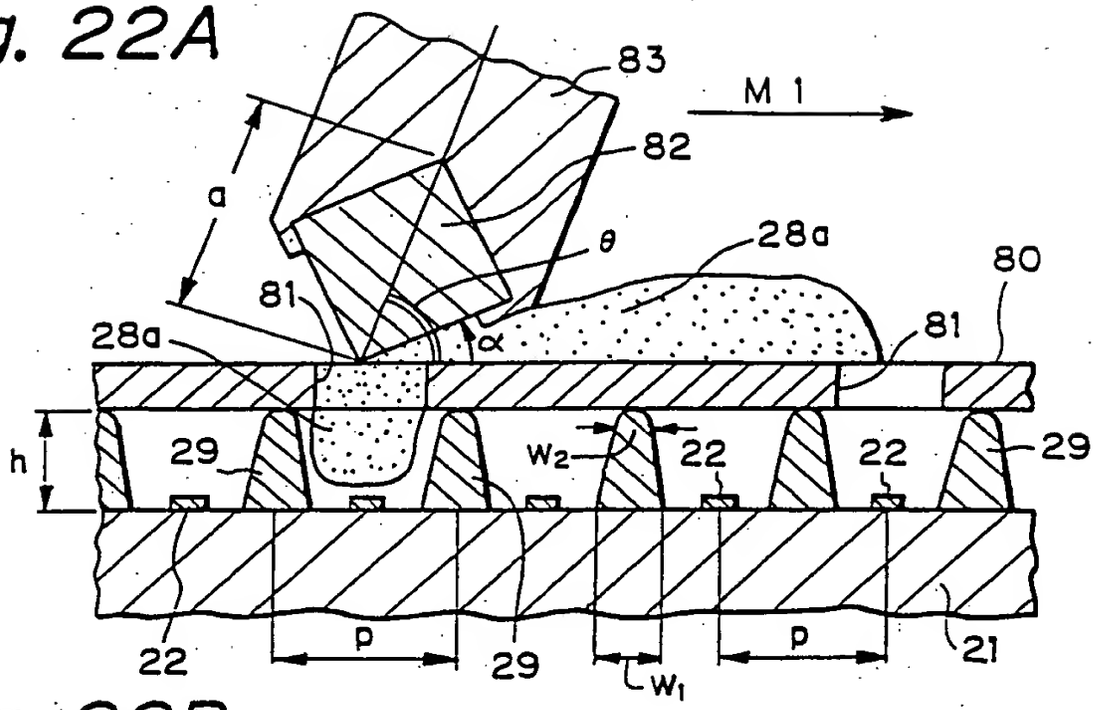

Fig. 22B

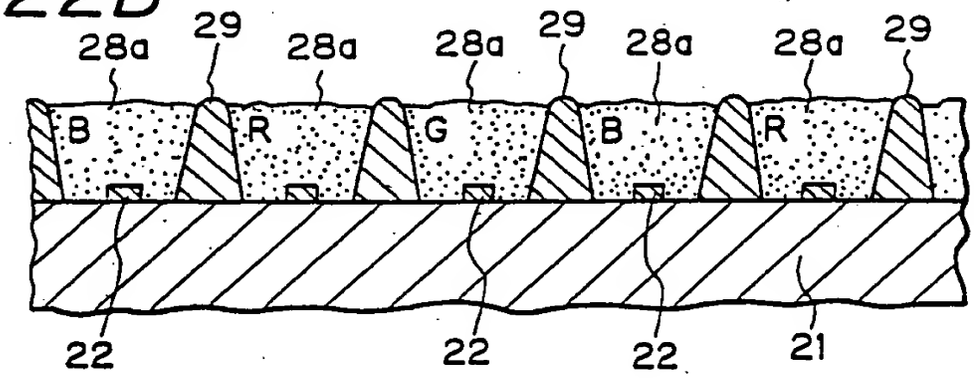

Fig. 22C

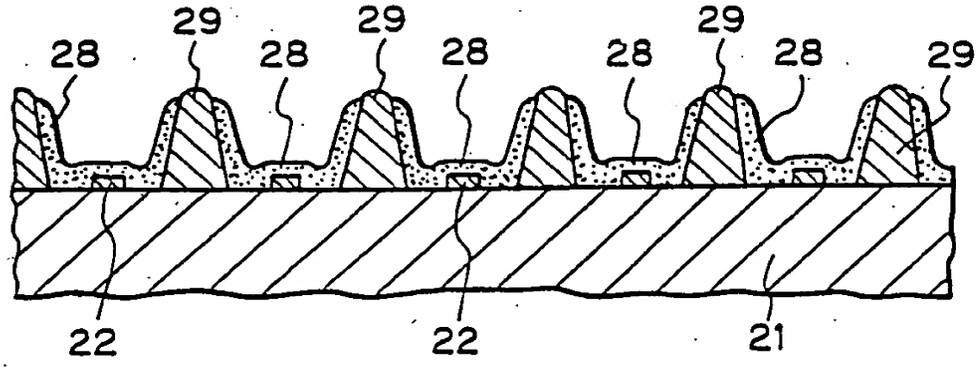

Fig. 23

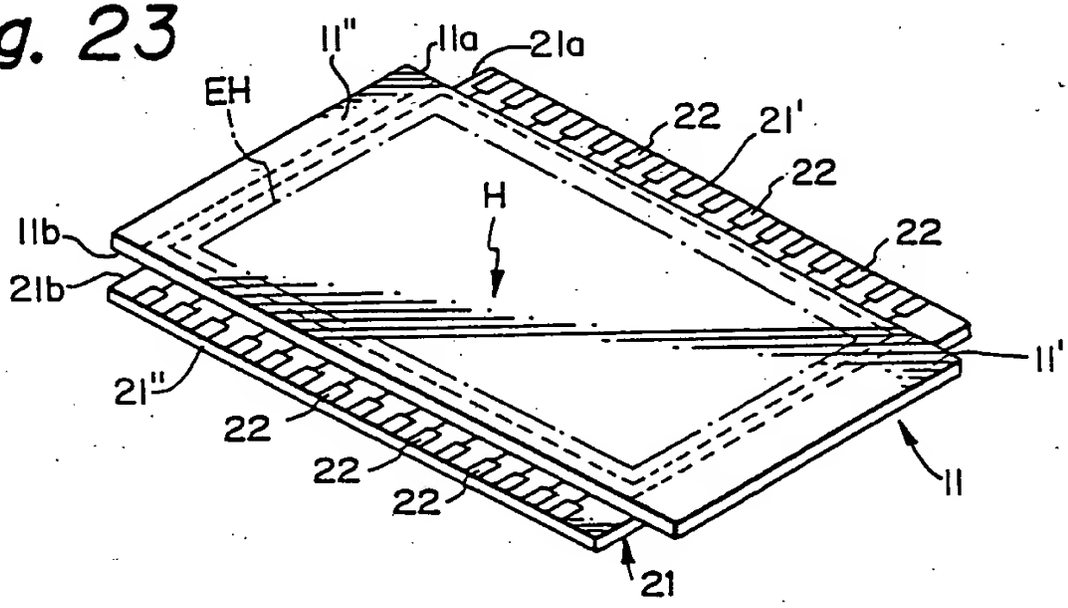

Fig. 24A
PRIOR ART

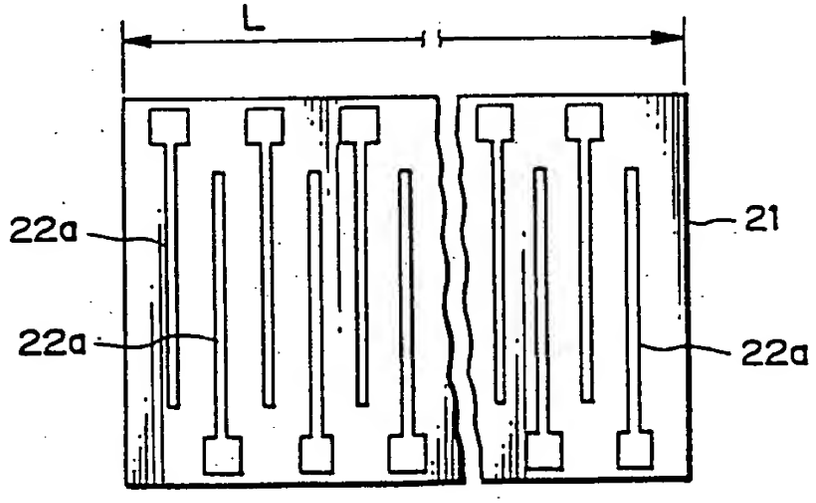

Fig. 24B
PRIOR ART

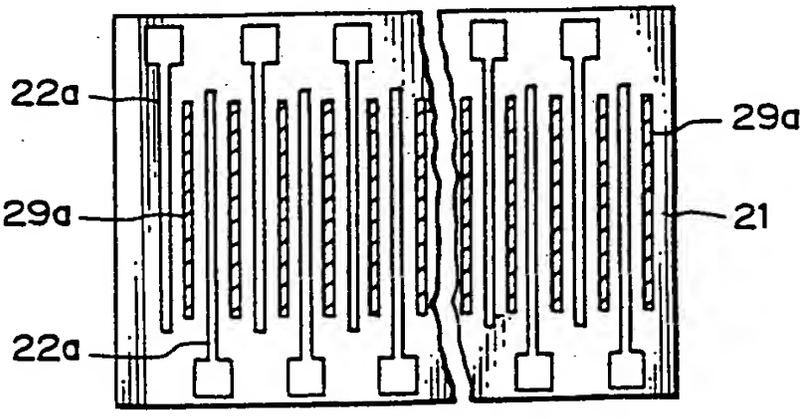

Fig. 25A

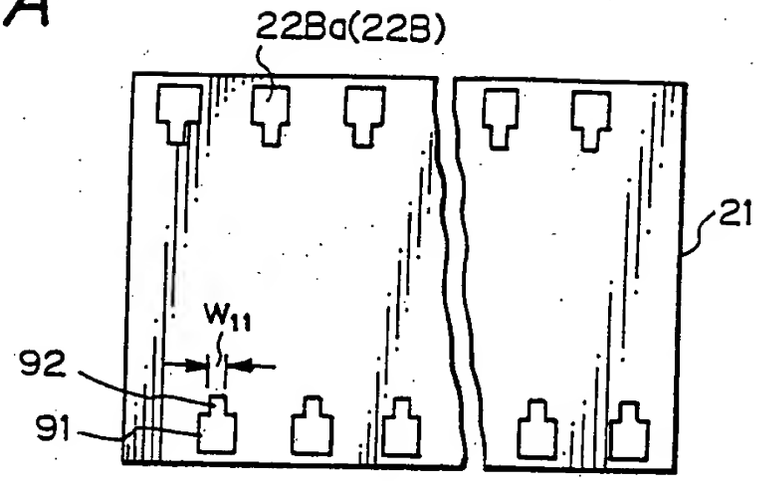

Fig. 25B

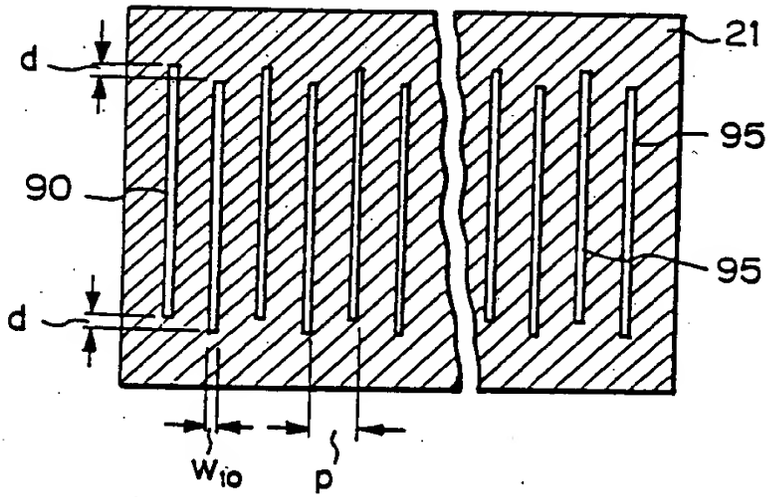

Fig. 25C

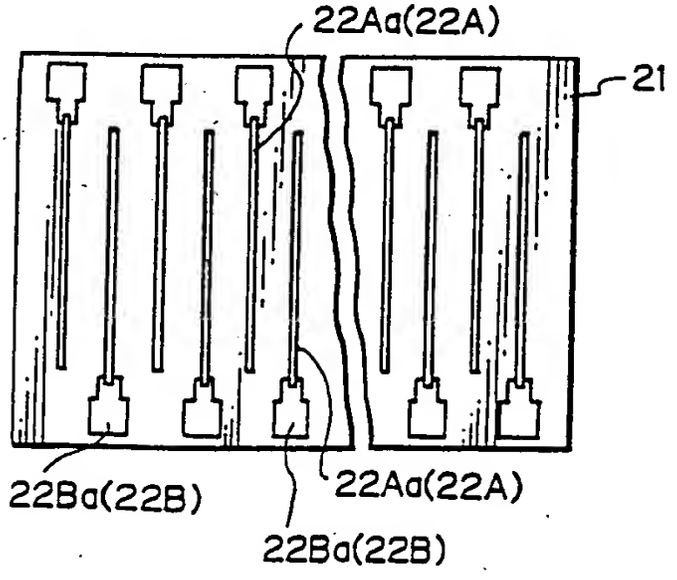

Fig. 25D

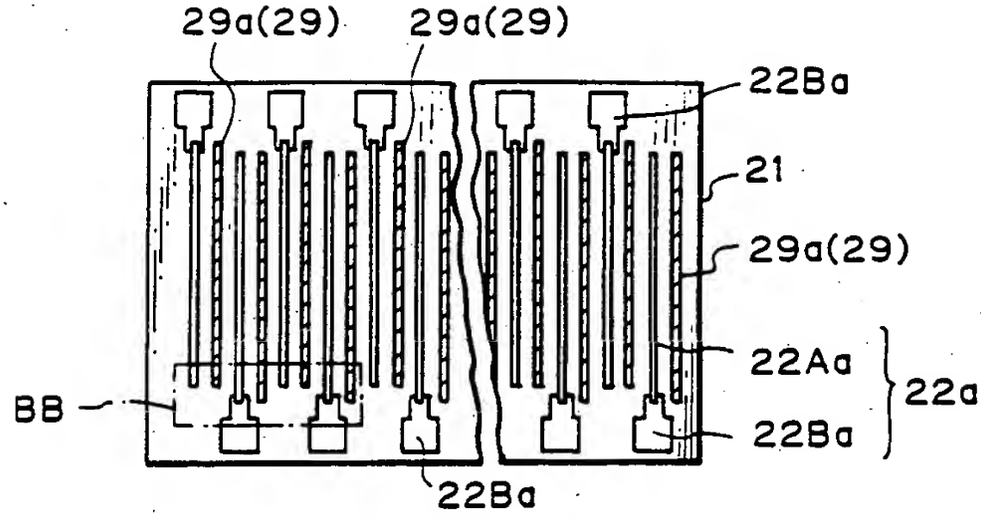

Fig. 25E